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Claims

[c1] 1. A low temperature polysilicon thin film transistor (LTPS-TFT) structure disposed on a substrate, comprising:
a cap layer disposed over the substrate, wherein there is a gap between the cap layer and the substrate;
a polysilicon film disposed over the cap layer, wherein the polysilicon film comprises a channel region and a source/drain region on each side of the channel region, and the channel region is directly above the gap; and
a gate disposed above the channel region of the polysilicon film.

[c2] 2. The LTPS-TFT structure of claim 1, wherein the structure further comprises a buffer layer sandwiched between the substrate and the cap layer so that the gap is disposed between the cap layer and the buffer layer.

[c3] 3. The LTPS-TFT structure of claim 2, wherein the gap has a coefficient of thermal conductivity smaller than the coefficient of thermal conductivity of the buffer layer.

[c4] 4. The LTPS-TFT structure of claim 1, wherein the gap has a coefficient of thermal conductivity smaller than the

coefficient of thermal conductivity of the substrate layer.

[c5] 5. The LTPS-TFT structure of claim 1, wherein the structure further comprises a gate dielectric layer disposed over the polysilicon film.

[c6] 6. The LTPS-TFT structure of claim 1, wherein the grain size of the channel region of the polysilicon film is on average greater than the grain size of the source/drain region of the polysilicon film.

[c7] 7. The LTPS-TFT structure of claim 1, wherein the width of the gate is smaller than the average grain size of the channel region.

[c8] 8. The LTPS-TFT structure of claim 1, wherein the gate comprises a dual gate structure.

[c9] 9. The LTPS-TFT structure of claim 1, wherein the structure further comprises:
a dielectric layer disposed on the polysilicon film and the gate, wherein the dielectric layer has a plurality of contact windows that exposes the source/drain region of the polysilicon film; and
a source/drain conductive layer disposed on the dielectric layer, wherein the source/drain conductive layer is electrically connected to the polysilicon film in the source/drain region through the contact window.

[c10] 10. A method of fabricating the channel layer of a low temperature polysilicon thin film transistor (LTPS-TFT), comprising the steps of:
providing a substrate;
forming a sacrificial layer over the substrate;
forming a cap layer over the substrate to cover the sacrificial layer;
forming an amorphous silicon film over the cap layer;
removing the sacrificial layer to form a gap between the substrate and the cap layer; and
melting the amorphous silicon film and the recrystallizing the melt silicon to form a polysilicon channel layer over the cap layer above the gap.

[c11] 11. The method of claim 10, wherein before the step of forming the sacrificial layer over the substrate, further comprises forming a buffer layer over the substrate.

[c12] 12. The method of claim 10, wherein the step of removing the sacrificial layer further comprises performing a wet etching operation with an etching solution having a higher etching rate on the sacrificial layer relative to the cap layer.

[c13] 13. The method of claim 10, wherein the step of melting the amorphous silicon film further comprises performing

an excimer laser annealing process.